R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicants' representative thanks Examiner Burd for the indication of allowable matter.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals. The second circuit may be configured to present the two or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-3, 9-12, 21 and 22 under 35 U.S.C. §102 as being anticipated by the background section of the present application is respectfully traversed and should be withdrawn.

In contrast to the background section, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a multi-phased first clock signal and (ii) two or more serial data signals. A second circuit may be configured to present the two or more serial data signals and the first multi-phased clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

The assertion in the Office action (see page 2, third paragraph) that any clock signal has "some" phase is not completely correct (see paragraph 7 of the attached declaration of Paul Scott). Phase is typically a measurement of a signal relative to some baseline (see paragraph 8 of the attached declaration). How can a signal have a phase with respect to itself? (See paragraph 8 of the attached declaration). Furthermore, the assertion that "the phase of the clock signal will be selected by the RXPLL before outputting the clock signal" is not supported by the background section (see paragraph 9 of the attached declaration). Box 22 of the background is a PLL that adjusts frequency to track incoming data (see paragraph 9 of the attached declaration). The background section is silent regarding phases of a clock signal (see paragraph 10 of the attached declaration). The background is also silent regarding a multi-phased clock signal (see paragraph 11 of the attached declaration). The background section does not show a plurality of phases of a clock signal (see paragraph 11 of the attached declaration). It follows that the background is silent regarding a selected phase of a plurality of phases of a first multi-phased clock signal, as presently claimed (see paragraph 12 of the attached declaration).

While the Office Action makes the assertion that "a new different phase will be selected by the PLL according to certain criteria, such as adjustments done in the PLL." However, a PLL typically adjusts frequency to manage phase (see paragraph 13 of the attached declaration). A typical PLL does not adjust phase.

The background section, on its face, does not disclose or suggest a selected phase, as presently claimed (see paragraph 14 of the attached declaration). In particular, none of the clock signals of the background section appear to be a selected phase of a plurality of phases of a multi-phased clock signal, as presently claimed. As such, the background section does not disclose or suggest the selected phase of the first clock signal.

In conclusion, the background section does not disclose or suggest a first circuit configured to present a parallel output data signal in response to (i) a selected phase of a plurality of phases of a first clock signal and (ii) two or more serial data signals. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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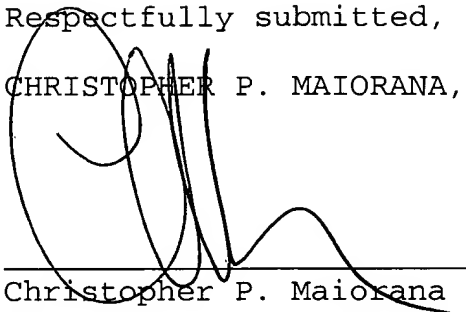

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